Design and implementation of a Cymbeline Radar signal processor with waveform generator to detect small RCS artillery bombs on a single FPGA chip

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Abstract— Cymbeline Radar is an old British mortar locating radar operating in x band using a Foster scanner. It has a nominal 100 kW peak output power using an old magneton, and a nominal pulse repetition frequency of 4000 pulses/second with 0.25 microsecond pulse width. It was built based on analog technology. This radar suffers from ageing, instability, in-coherency, poor accuracy, and difficult maintenance. In the present work, a proposed modified version of this radar is introduced. The proposed version depends on changing the radar parameters such as peak power, pulse width, and waveform generation and processing based on advanced technologies. A 6 KW Traveling Wave Tube (TWT) is suggested with a transmitted waveform of 6 microsecond pulse width and Barker code modulation. The same pulse repetition frequency is used. These parameters are chosen to achieve the designed radar specifications with an enhanced performance, and available technology The waveform generation and signal processing is achieved using Field Programmable Gate Arrays(FPGA's) which are best suited for signal processing applications that requires real time processing. The proposed signal processor includes matched filter and pulse compression with side lobes cancellation, Moving Target Indicator (MTI), Doppler processing, and Constant False Alarm Rate (CFAR) processing.

Keywords— Radar; Matched Filter; Barker code; FPGA; MTI; CFAR; Pulse compression.

I. INTRODUCTION

In the modern radars the improvement in target detection can be achieved using modulating waveform. A Radar with pulse compression technique transmits a special waveform and make processing on the received echo to achieve the required range resolution. In our designed radar we have achieved reduction in power from 100Kw up to 6Kw. Obtaining better range resolution. Maximization of signal to noise ratio can be obtained using matched filter which convolutes the reference signal which is stored on a memory with the received one from the target. Achieving the required range resolution can be by comparing the main lobe width and the sidelobe levels. One of the disadvantages of pulse compression technique is increasing in sidelobe level which can be reduced also by matched filter or cancelled by sidelobe suppressor. Through the processing the radar gains high signal to noise ratio, maximum range, high resolution and high immunity against radar jamming or interference.

II. WAVEFORM GENERATION

There are different types of waveforms in radars which may be continuous or pulsed. To achieve maximum range we chose pulsed waveform which is modulated either LFM or Barker but in our design we generate binary phase coded (Barker) .An ordinary Cymbeline radar uses a pulse of 0.25microsecond width and 0.25 mms pulse repetition period which needs high peak power up to 100KW which is very cost and needs large transmitter but in our design using nested barker code (3/3/3) which achieves almost the same required maximum unambiguous range but with better range resolution which can be calculated by…

$$\delta R = \frac{C*\delta 1}{2} \quad (1)$$

Where $\delta 1$ is the sub pulse width which is equal to 0.2 us

C is the speed of light

So Range resolution has been improved to 30 m.

The minimum range can be calculated using the pulse width which equals 5.4 us which achieves 810 m minimum range.

$$Pav = \frac{Pt*\delta}{Tr} \quad (2)$$

So for a peak power only 6 KW we can achieve 160 watt average power.

From this pulse compression technique, the maximum range that our designed radar can detect can be calculated by Radar range equation which is

$$Rmax = \sqrt[4]{\frac{Pt*G^2*\lambda^2*\sigma}{(4\pi)^3*Noisefloor}} \quad (3)$$

Where Noise floor =K*T0*B*F+SNR proc dB

So, for the following parameters:

G=30 dB

F=9.6 GHz

L=10 dB

SNR proc =6 dB

We can achieve up to 11.5 Km maximum range.

Increasing the length of nested barker, increasing the range resolution and improve signal to noise ratio but this has a bad effect on sidelobe which is the main disadvantage pulse compression which increasing sidelobe level but this problem can be solved using sidelobe suppressor which is optimum filter using to remove sidelobes and maximize signal to noise ratio which will be discussed later. Now we discuss how generation the waveform will be on FPGA, firstly generate the MATLAB code (m.file) and make its coefficient file then using memory (ROM) IP core on ISE Xilinx we store the coefficient file, secondly using counter to control the length of Tr to 1024 samples, third change from fixed to float 32 bit then to DAC 10 bit then to transmitter and figure (1) is the schematic of waveform generation:

Storing the transmitted pulse is to be used again when receiving the echo to make a convolution to make the matched filter processor.

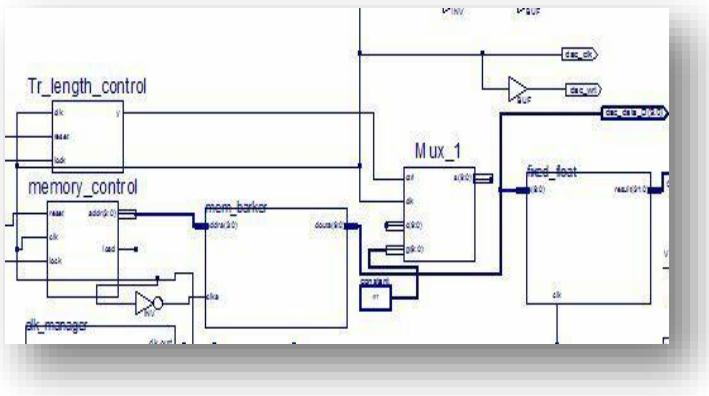

Fig.1. schematic of waveform generator

III. Matched filter

The matched filter, shown in Fig.(2) is a processor to maximize signal to noise ratio ,it is the autocorrelation function of the transmitted pulse ,it is a filter whose response h(t) is the reverse of transmitted signal with shifting in time where h(t)= x(t-s).But it is implemented in frequency domain by taking the FFT of replica and the conjugate FFT of transmitted pulse which is stored previously on a memory (ROM) , then using a complex multiplier to calculate the output of matched filter in frequency domain by taking the FFT of replica and the conjugate FFT of transmitted pulse which is stored previously on a memory (ROM) , then using a complex multiplier to calculate the output of matched filter in frequency domain . The inverse FFT (IFFT) is used to transform the output to a time domain and take the absolute value. MF response is shown in Fig.(3).

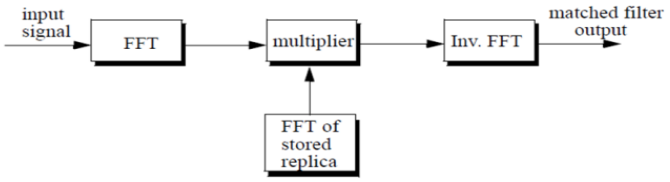

Fig.2. Block diagram of matched filter

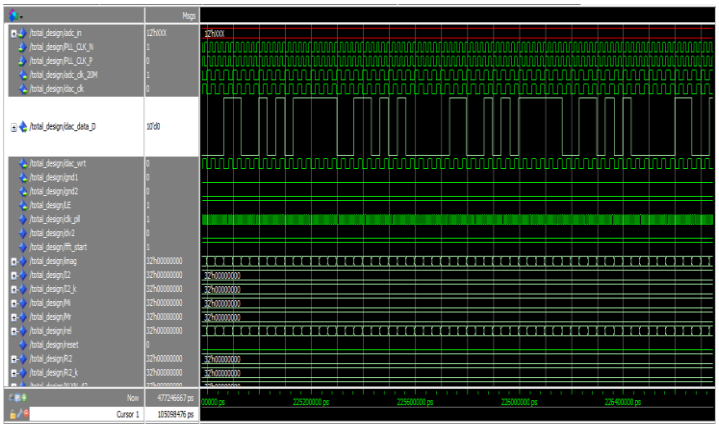

Fig.3 The response of matched filter

D. Sidelobe suppressor (SLS)

The optimum filter is a filter whose impulse response is equal to the spectrum of the correlation function of the transmitted signal without time-side lobes divided by the spectrum of the correlation function of the transmitted signal.

The advantage of the optimum filter over other side lobe reduction methods is that it doesn't reduce the amplitude of the time-side lobes but it completely suppresses it, another advantage over the mismatch filter is that it doesn't affect the amplitude of the input signal therefore no bit growth in the word length at the filter output and no extra hardware resources is required after the optimum filter due to bit growth.

The frequency response of the optimum filter for Barker 13 is given by for an N length sequence:

$$\omega(k) = \frac{\pi k}{\frac{N}{2}} \tag{4}$$

$$H(k) = \frac{N}{N + 2\sum_{i=1}^{\frac{n-1}{2}} \alpha(i) \cos 2i\omega(k)} \tag{5}$$

IV. Moving target indicator (MTI)

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The main purpose of MTI whose schematic is shown in Fig.(4) is to cancel the fixed targets or slightly moving targets due to clutter such as rain, fog and trees. The simple MTI is a single delay canceller. The MTI is designed using 2 blocks of shift registers whose depths are equal to the number of range cells in each repetition period.

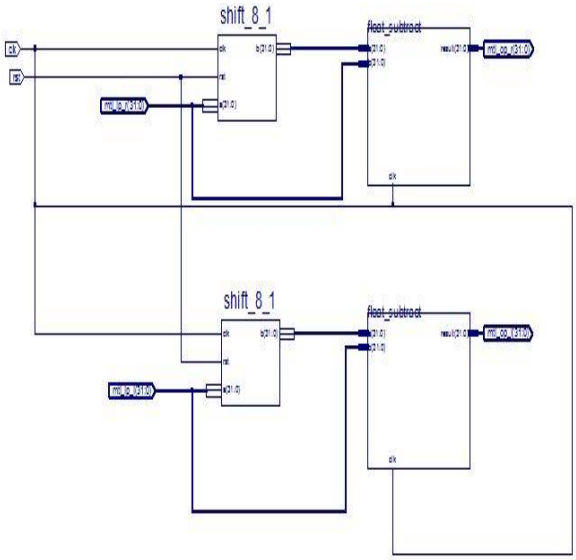

Fig.4. MTI schematic using FPGA

V. CFAR

A CFAR, whose schematic is shown in Fig. (5), is a processor for detection of targets in presence of noise and clutter. The CFAR establishes a mean level estimate (MLE), based on a range sample of the clutter signal near the target cell. The MLE is used to adjust the processing thresholds to minimize false alarms. The main concept of CFAR is it takes two windows around the target cell and two guard cells since the echo may be wide so it occupies more than one cell, then taking the average of each window and taking the average of the output of two windows, then by applying to a comparator to compare with the target and guard cell we can detect if the echo is target or not. CFAR response is shown in Fig. (6).

VI. Hardware implementation

This design is implemented on FPGA chip which has 10-bit DAC and 14-bit ADC and two differential clocks.

Fig. (7) is a real hardware implementation in low complexity. The main advantage of Sidelobe suppressor is cleared in CFAR, without SLS in nested barker which increases the length so we need a CFAR with larger width to compensate the sidelobe level than using SLS which eliminate the sidelobes. Fig.8 shows the measured Binary phase modulating waveform.

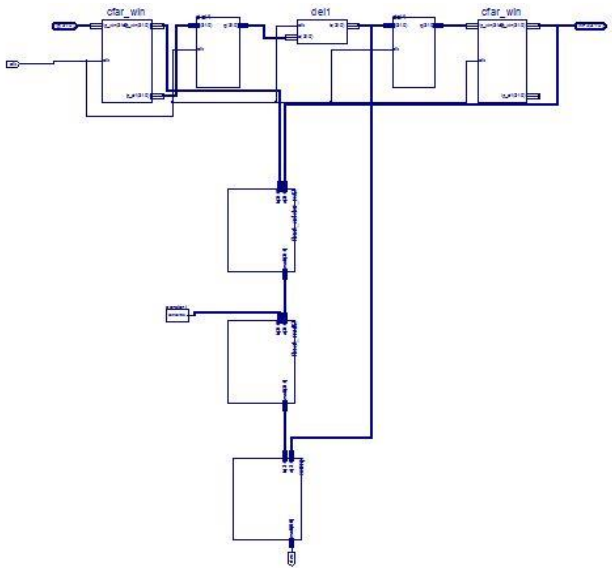

Fig.5. CFAR schematic using FPGA

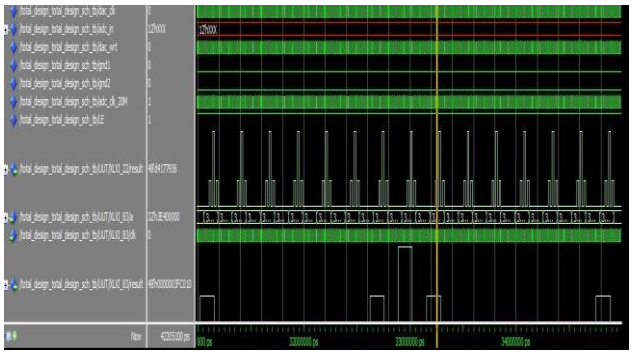

Fig.6. Output of CFAR processor

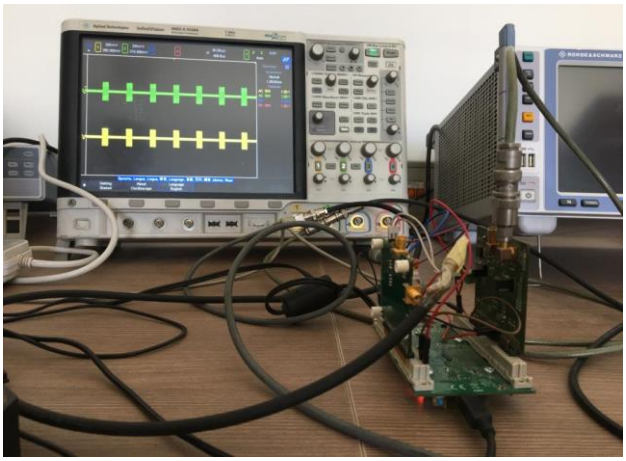

Fig.7. Real image of hardware in lab

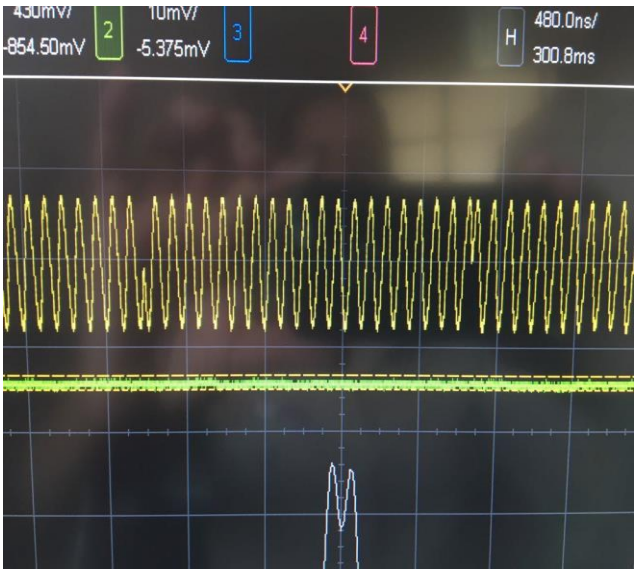

Fig.8. Binary phase modulating waveform

VII. Conclusion

There is an approach which is used in our designed radar which is the binary phase modulated barker pulsed waveform. This pulse compression technique is used to reduce the peak power while maintaining the average power constant. The average power is the effective power to determine the maximum range which radar can detect.

Using nested Barker (3/3/3) we achieve required maxim range with better range resolution reduction in peak power up to 6KW. Design the corresponding matched filter and CFAR integrator which are the main methods to enhance the detection capability of targets in presence of noise and clutter. The following table shows in brief the improvement that achieved in our designed Radar.

Table.1. Comparison between old and the new designed Radar

Type of comparison	Old Cymbeline Radar	Our designed radar
Waveform type	Simple pulse with 0.25 us pulse width	Binary phase modulated nested Barker (3/3/3) waveform
Transmitter type	Magnetron	Travelling wave tube (TWT)
Peak and average power	100 kw(peak), 100 w (average)	6Kw (peak) ,160 w (average)
Range resolution	40 m	30 m
Rmax unambiguous	37.5 Km	30.7 Km

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