Design and generation of 50 kHz and 200 kHz pulsed sine wave using FPGA

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Abstract– in this paper, design and generation of 50 kHz and 200 kHz is proposed using FPGA VHDL codes. The type of FPGA Board used in this project is Altera DE1-SoC. Altera DE1-SoC development kit comprises of Cyclone V SoC 5CSEMA5F31C6 device and has 85K Programmable Logic Elements which are more than sufficient for this project. The trigger starts the process of generation of pulses of desired frequency and duration. The pulses are generated through Pulse Width Modulation (PWM) technique. The designed pulses have PRF of 10 Hz to get maximum depth of 75 m and have pulse length of 0.4 mS to get good resolution of 0.3 m. The bandwidth designed is 5 kHz for 50 kHz and 200 kHz signals. Codes are flexible to generate other signals with different frequencies and different PRF. The simulation is done using Modelsim software which is also a tool form Altera used for simulation and debugging of the digital logic. It is used to check the timing requirements. Their combination results are efficient to be amplified and then transmitted using transducer.

Keywords—50 kHz pulsed signal, 200 kHz pulsed signal, VHDL codes, Altera FPGA, Optimum range resolution

I. INTRODUCTION

After the Analog Front End, there has to be a digital part which can process the signal and use it for displaying, saving or editing afterwards. Earlier in digital Electronics, the trend was to use a set of specialized discrete logic circuits, to obtain specific outputs. In order to create a slightly complex design, one needed to add few tens of such chips on a single board. This resulted in complex board layout and reduced performance. To improve performance, programmable logic method was introduced.

A. FPGAs

FPGAs are digital integrated circuits (ICs) that contain configurable blocks of logic along with configurable interconnects between these blocks. Depending on the way in which they are implemented, some FPGAs may only be programmed a single time, while others may be programmed over and over again. The term "Field Programmable" implies that the device is programmed by the customer i.e., in the "field" and not by the manufacturer. The advantage of using FPGAs over CPLDs is that the former can be implemented for complex designs and based on Look-up tables (LUTs) while the later ones are for simpler designs.

B. *VHDL Development*

After the board was built and simulation was done, it was time to check the operation of various components practically. For this purpose, it was necessary to communicate with the hardware and this was done using the VHDL language in Quartus. To make the software development easily accessible and editable for future use, the code development part was done in certain steps depending upon the components on the board to be driven.

II. Pulse Generation

A. Clock divider

DE1-SoC board has four 50MHz clock signals connected to the FPGA which can be used as clock sources for user logic. a high frequency clock is not required in this project, so a clock divider logic was developed which divides the 50MHz clock down to 5MHz. ADC deals with inputs having frequencies in kHz range like 50, 200kHz. By providing a clock of 5MHz, these frequencies are sampled with a sampling rate which is much higher than the Nyquist frequency and thus gives a better resolution. Similarly, DAC also operates on 5MHz clock but it needs a greater number of clock cycles to transfer a digital value as compared to ADC. Still, 5MHz clock is sufficient.

B. Generation of signals

The pulse generation process starts with OE going High (’1’) from Low (’0’). The position of the Switch SW0 determines the frequency of the pulses. Here, high value of SW0 gives out 50kHz pulses and low value gives 200kHz pulses. The amplitude of these pulses toggle between 0 and 3.3V as available from the GPIO Header. When a certain number of cycles are produced, the inputs return back to their Initial values and OE also goes low thus, disabling the outputs. After each pulse train is produced, the system goes to the Idle state.

C. State Machine

Next is the state machine describing the VHDL code for pulse generation. The inputs INA and INB are initially set to

be ’0’ and ’1’ respectively. The pulse generation process starts with OE going High (’1’) from Low (’0’). The position of the Switch SW0 determines the frequency of the pulses. Here, high value of SW0 gives out 50kHz pulses and low value gives 200kHz pulses. The amplitude of these pulses toggle between 0 and 3.3V as available from the GPIO Header. When a certain number of cycles are produced; the inputs return back to their Initial values and OE also goes low thus disabling the outputs. After each pulse train is produced, the system goes to the Idle state. Then, the same process is followed again to produce the next burst number of cycles are produced; the inputs return back to their Initial values and OE also goes low thus disabling the outputs. After each pulse train is produced, the system goes to the Idle state. Then, the same process is followed again to produce the next burst.

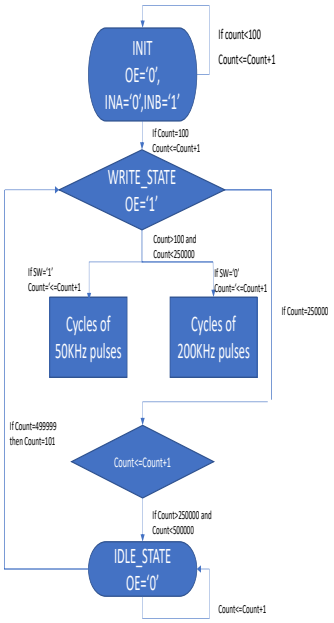

Figure.1 State Machine for generating 50 and 200kHz pulses

III. Implementation And Design

Electrical pulses are generated using digital logic before converting them into acoustic pulses with the help of a transducer.

For generating the electrical pulses, there should be a trigger pulse present which decides the rate at which pulses will be fired from the echo sounder. It is also called Pulse Repetition Frequency (PRF) and is important because it must always occur at a precisely defined interval of time. PRF depends on the depth of water to be surveyed i.e., time interval long enough between pulses so that all the echoes resulting from first transmission have returned, before the next transmission. Otherwise, it will affect the echo sounder’s proper operation.

The time interval between the successive bursts is decided by the sound’s velocity in water, c and the total distance traveled by the pulse i.e., with increasing distance, the time between bursts will increase.

The expression is given by:

$$Time = 2*depth/c \qquad (1)$$

Let depth = 75m. Therefore, Total distance traveled = 150m

So,

$$Time = 150/1500 = 0.1sec$$

It means that time interval between successive bursts should be around 100ms.

$$PRF = 1/Time\_Interval \qquad (2)$$

Therefore, Maximum PRF should be 10Hz or 10 bursts per second.

The trigger starts the process of generation of pulses of desired frequency and duration. The pulses are generated through Pulse Width Modulation (PWM) technique. These Square wave pulses have a 10% duty cycle i.e., each pulse, for half of the time it is in positive cycle and in the next half it is in the negative cycle. These electrical pulses usually have a defined frequency like 50, 70 or 200kHz and their duration is decided by the number of cycles. This pulse duration is called tau (τ) and is usually in the range .1-.5ms for better resolution. So, for a 50kHz pulse the number can be between 5-25 cycles.

When this τ is multiplied by C / 2, range resolution is obtained. Range resolution is important to determine the minimum distance between targets i.e., between two fishes, so that their reflected echoes do not overlap each other and can be prevented from being shown as a single signal at the receiver end. Therefore, with smaller τ, better resolution can be achieved.

The duration of pulses is set according to transducer’s bandwidth and a fixed number of cycles are chosen so as to make a particular pulse duration, 20 cycles of 50kHz will have a pulse duration of .4ms which will make a pulse length (c* τ) of 0.6m in the water. Similarly, for 200kHz frequency, the number of cycles has been changed to 80 so as to have the same pulse duration and length.

Both the operational frequencies i.e., 50 and 200 kHz can be achieved by just toggling the Switch (SW0) present on the

DE1-SoC board, with SW= ’1’ for 50kHz and SW= ’0’ for 200 kHz as described in the code.

IV. Simulation Results

Simulation is a very good method for understanding the operation of various components and getting the better results faster without spending so much time. By performing simulation, it becomes easy to locate the error in the code as the outputs can be seen visibly. For this purpose, Spice was used for testing the amplifier and Modelsim for the digital code. The duration of pulses is set according to transducer’s bandwidth and a fixed number of cycles are chosen so as to make a particular pulse duration. 20 cycles of 50kHz will have a pulse frequency, the number of cycles has been changed to 80 so as to have the same pulse duration and length.

The 200 kHz pulsed sine wave code is simulated Modelsim and write state types are as show in figure 1.

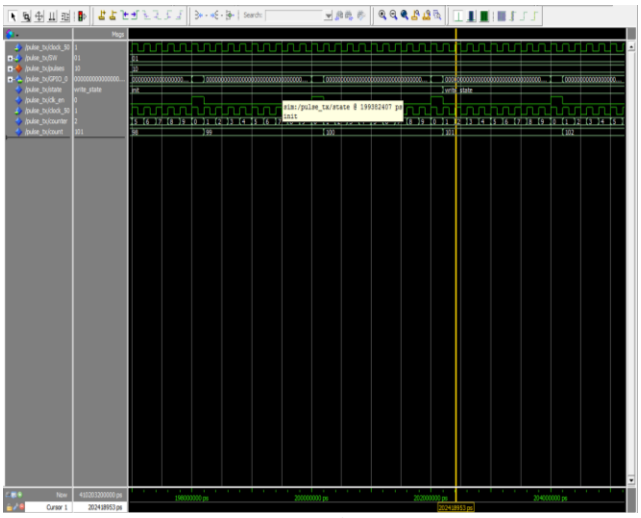

Figure.1 The Simulation of 200kHz Using ModelSim

In addition, the 200 kHz pulsed sine wave code is simulated Modelsim showing write state as in figure 2.

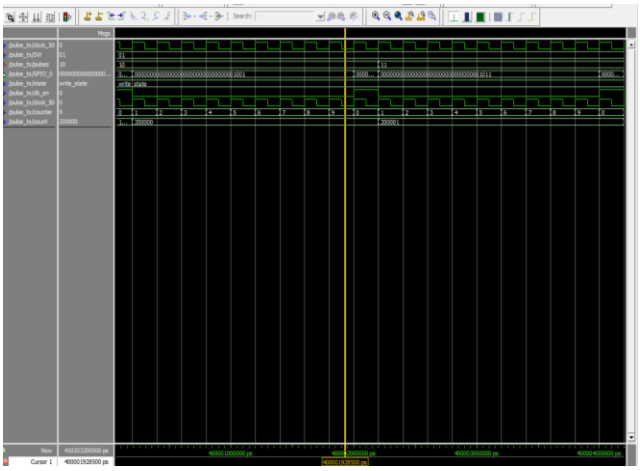

Figure.2 The Simulation of 50kHz Using ModelSim.

The designed codes are also simulated using Modelsim for calculating no of sub-pulses generated for both 50 kHz and 200 kHz. The results show different state type including the generation of the signal. These results of the sub-pulses generated in one pulse are showed in figure 3.

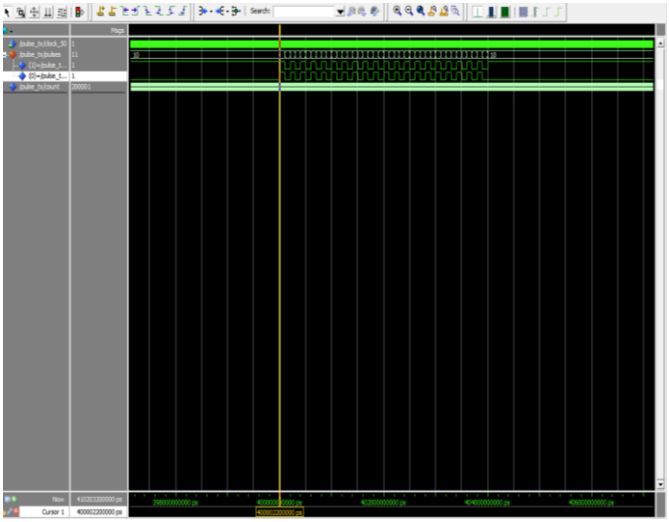

Figure.3 sub-pulses generated in one pulse for both 50 kHz and 200 kHz

Then the VHDL codes are uploaded to the FPGA using Quartus prime software and the generated pulses are measured using an oscilloscope as shown in the following figures 3.

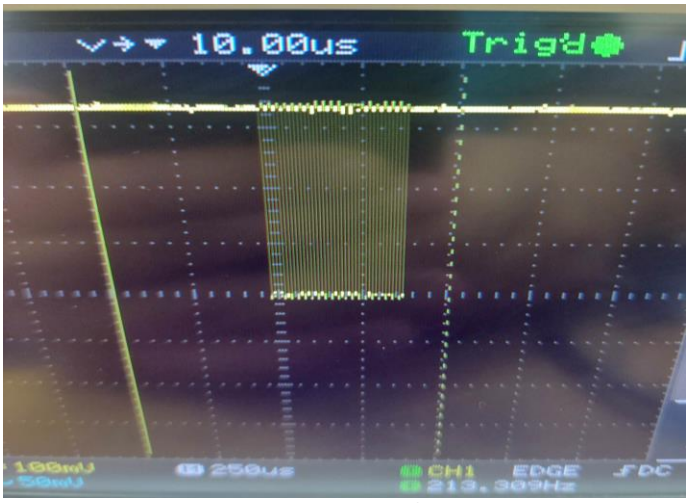

Figure.3 sub-pulses generated in one pulse for 50 kHz on oscilloscope.

Also, the pulse width of pulses generated is measured using oscilloscope which is 0.0004 us. The result shown in figure 4 show the accurate generated pulse width.

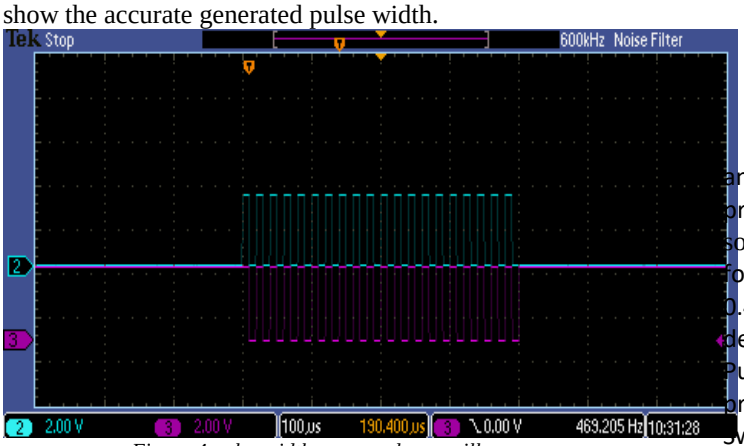

Figure.4 pulse width measured on oscilloscope.

For accurate measurement of frequencies of generated pulses, a spectrum analyzer is used for measuring. The results are shown in figure 5,6.

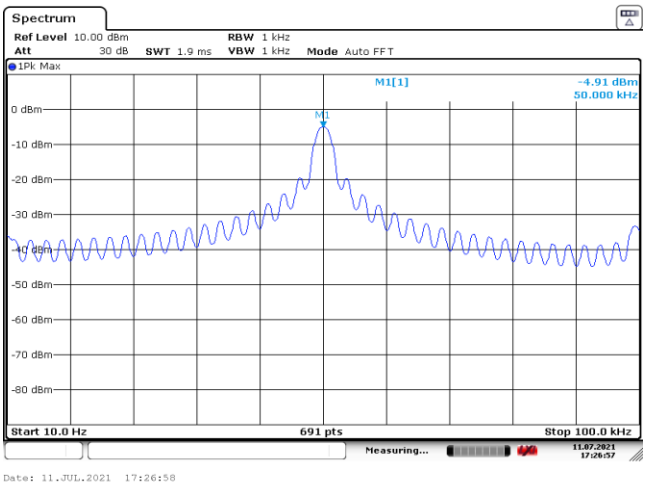

Figure.5 Frequency Spectrum of the 50 KHZ Using Spectrum Analyzer

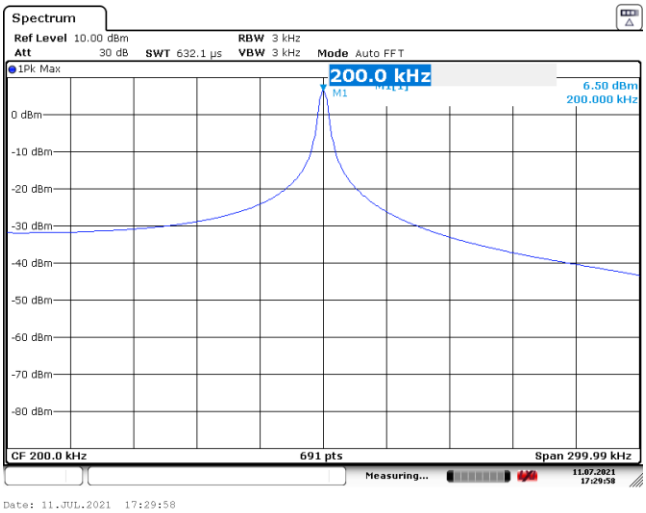

Figure.5 Frequency Spectrum of the 200 KHZ Using Spectrum Analyzer

Conclusion

The code of Generated pulses with frequencies of 50 kHz and 200 kHz is written by VHDL language and will be programmed using Quartus II which is a programming software tool by Altera. The pulses generated has a 10 Hz PRF for maximum depth of 75 m. The pulse width of the pulses is 0.4 mS to get a range resolution of 0.6 m. The VHDL code designed are flexible for changing both frequency and PRF. Pulses of two different frequencies can be generated and processed by the receiver by just toggling the position of switches on the FPGA board. Thus, the user has a large control over the signal processing which is basically important for the echo sounder systems developed for research purposes.

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