Design and Implementation of Time Variable Gain Amplifier (TVG) using FPGA

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Abstract– In this paper, design a time variable gain control is proposed using FPGA VHDL codes. For echo sounder and sonar systems, it is necessary to amplify the returned echo from the targets. Using the Altera DE1-SoC development kit for controlling the gain control pin of the amplifier make it flexible to do more than one process on same board. The algorithm used in this paper make it easy for changing the value of each step of TVG. TVG VHDL code is designed for 0.1 mS period pulse with 10 Hz. Also, considering the effect of high amplitude echo with high delay time on receiver saturation, the algorithm is designed with hold state for avoiding this effect. The TVG code timing is synchronous with the transmitted signals. The VHDL code is designed using Quartus software and being simulated using Modelsim software. Their combination results are efficient to be used for controlling Digital to Analog Converter (DAC) amplifier which used to generate amplified signal.

Keywords—Time variable gain, TVG amplifier, TVG VHDL code, FPGA, Receiver saturation, DAC

I. INTRODUCTION

To provide the necessary gain to the echo signal, an amplifier is needed. This can be achieved by providing fixed amplification as implemented by Dr. Balk [1] using Op-amps and discrete components in its various channels. But it is desired to have a digital control over the gain range. Therefore, it is advantageous if an amplifier is used whose gain can be changed digitally using FPGA.

A single amplifier can provide the necessary gain but the Bandwidth will decrease accordingly with gain due to the Gain-Bandwidth (GBW) product. So, it is practical to use more than one amplifier to raise the low amplitude echoes. Connecting amplifiers in series, where each amplifier sends its output to the input of the next amplifier is the technique used for amplification. This also improves the attenuation of out-of-band interferes, since cascaded stages have a sharper high-frequency roll-off for the same effective gain-bandwidth product, compared to a single-stage amplifier [2].

As stated above, the gain required should be large enough so that output voltages are in the operating range of ADCs. To achieve this goal, the number of cascaded amplifiers needs to be chosen according to the gain required. A large number of amplifiers are available from different vendors. But only the amplifiers with the variable gain characteristic should be used for this purpose. This is because echoes from targets i.e., fishes at different depths will require different gain due to different ranges covered by the signal. As the intensity of the signal falls directly with the distance traveled and thus, with time. Therefore, Variable Gain should be dependent upon time i.e., the purpose of applying Time Variable Gain (TVG) here is to reduce the dynamic range of echo signal and adapt it to the dynamic range of the ADC [3].

A. FPGAs

FPGAs are digital integrated circuits (ICs) that contain configurable blocks of logic along with configurable interconnects between these blocks. Depending on the way in which they are implemented, some FPGAs may only be programmed a single time, while others may be programmed over and over again. The term "Field Programmable" implies that the device is programmed by the customer i.e., in the "field" and not by the manufacturer. The advantage of using FPGAs over CPLDs is that the former can be implemented for complex designs and based on Look-up tables (LUTs) while the later ones are for simpler designs.

B. *TVG Generation*

TVG is accomplished by generating a voltage waveform of a defined wave shape and applying it to the receiver amplifier. The TVG can be controlled either digitally or by analog voltage. For ease of adjustment, TVG action can be obtained by different methods such as:

A) TVG Using Capacitor

TVG action can be obtained by charging a capacitor with a negative voltage during the transmission cycle, and after this cycle, discharging the capacitor through a shunt resistor. The over-bias voltage then decays exponentially to the normal bias level. Thus, the amplifier is designed to have a gain in dB that is approximately linear with the bias voltage [4].

B) TVG Generated Digitally

It is more accurate to provide the TVG digitally with the help of a Digital to Analog Converter (DAC) or Digital Potentiometer. A precise TVG can then be achieved and changed accordingly with range and incoming signals. The output analog voltage from DAC can then be given to the variable amplifier as gain control voltage.

This TVG should compensate for the following Transmission Loss (TL) vs. Range curve.

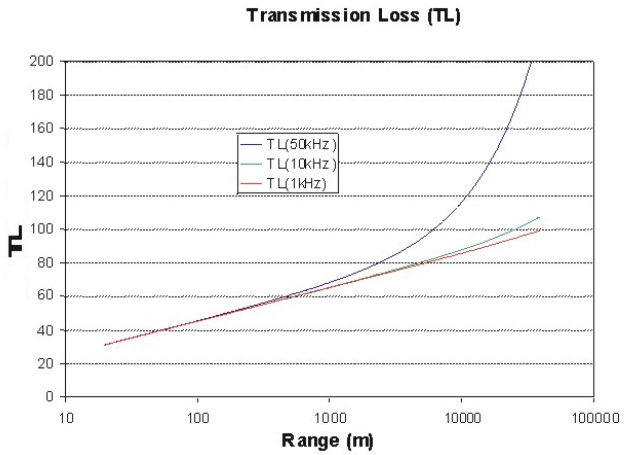

Figure 1: Transmission Loss vs. Range [5]

For the ultrasound systems, all the amplifiers require a common analog voltage for gain control and it becomes easier to achieve gain with a single control voltage routed to each VGA.

C. Transmission loss and Power Calculations

The acoustic pulse while traveling through the medium experiences Transmission Loss (TL). This loss is mainly due to spreading and attenuation. The spreading loss is a geometrical effect representing the regular weakening of a sound signal as it spreads outward from the source and this loss increases with the range. This affects the signal's strength and as a result, the echo which is received has a very low amplitude. Therefore, this loss needs to be compensated.

The transmission loss responsible for the weakening of the pulse strength is given by the equation:

$$\mathbf{T\,L = 20Log\,(R) + aR} \qquad \mathbf{(1)}$$

where **α** is the absorption coefficient and 20Log(R) is the spreading loss.

As **α** depends on frequency, it will have different values at different frequencies, E.g., α for 50 and 200kHz is 0.009dB/m and 0.05dB/m respectively for long distance (R=100m), Transmission Loss is calculated out to be:

For 50 kHz: TL = 40.9 dB

for 200 kHz: TL = 45 dB

III. Implementation And Design

A. Design Of AD605 Circuit.

Amplifying incoming echo from targets has many ways. One way of this ways is using Variable gain amplifiers are easily available but there are some requirements which help in filtering out the unnecessary amplifiers. It is desired that those amplifiers can provide a gain range from 0 to around 90 decibels(dB). The bandwidth should also be large for different gains. Among available choices amplifier like AD8338 [6] from Analog Devices was a good choice. It can provide gain up to 80dB with 18MHz Bandwidth. It was not used because it offered a slightly higher Input noise.

Amplifier AD605 [8] is used in this project. AD605 is a low noise, differential-input, dual-channel, linear-in-dB Variable Gain Amplifier. It fulfills the desired characteristics of gain, noise, supply voltage etc. It comprises of two variable gain amplifiers which can be connected in series to get higher gain ranges, up to 96dB and it uses a common gain voltage (*VGN*) for both the amplifiers to control the variable gain.

The gain scaling for this amplifier can be set between 20dB/V and 40dB/V with the help of VREF pin for better gain scaling. Providing VREF 2.5V will set the scale factor to be 20 dB/V while 1.25V will set it to 40 dB/V. Accordingly, the gain scales linearly in dB with control voltages (*VGN*) of 0.1V to 2.9V for the 20 dB/V scale and 0.2V to1.2V for the 40dB/V scale. The amplifier can be used with differential/single-ended inputs and the output is single-ended. The negative inputs of both the channels are connected to the ground through 0.1¹F ceramic capacitors if it is used as a single ended amplifier. Figure 2 shows the circuit design for amplifier AD605.

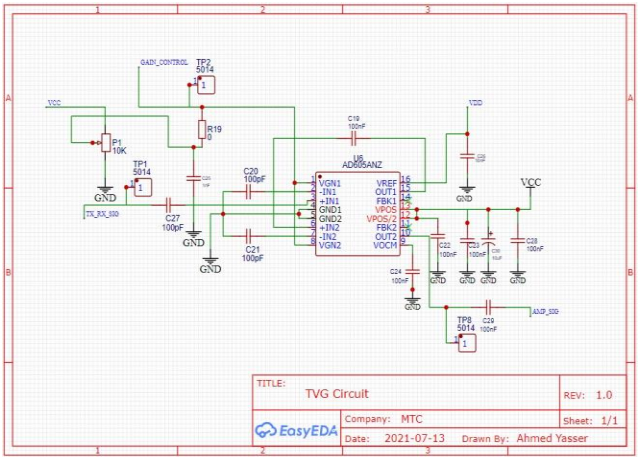

Figure 2: Circuit Diagram of AD605.

For the ultrasound systems, all the amplifiers require a common analog voltage for gain control and it becomes easier to achieve gain with a single control voltage routed to each VGA. So, figure 3 shows the connection of digital-analog converter [9] used to convert the digital output of FPGA into analog signal for controlling the amplifier.

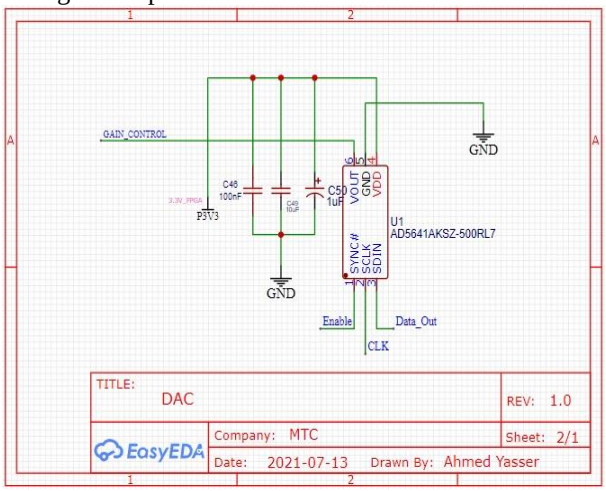

Figure 3: Circuit Diagram of DAC.

B. Design Of TVG VHDL code.

The following state diagram show how the VHDL code work as ramp control from 0 up to 2.9V then hold maximum value of 2.9V to avoid saturation of the receiver. This process is repeated with PRF of 10Hz so this process happens within a time interval of 100ms.

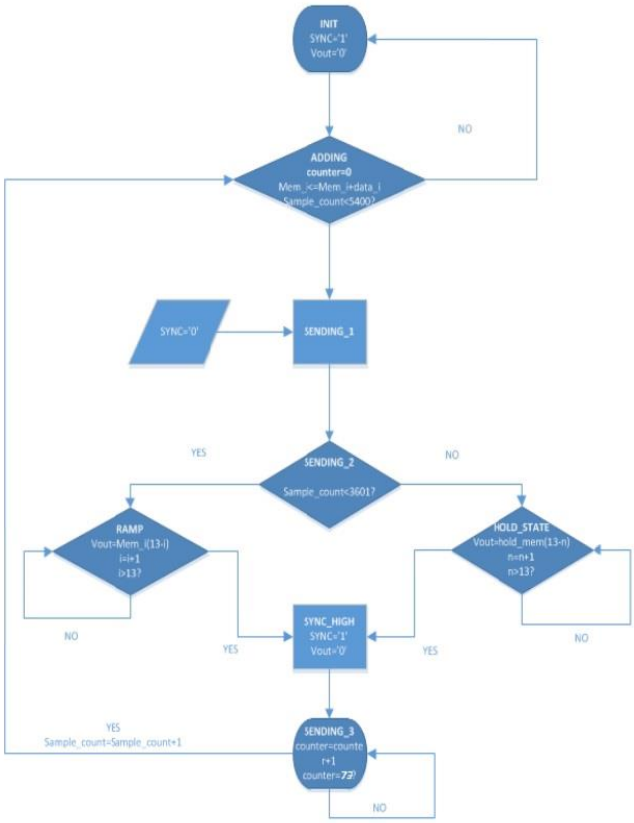

Figure 4: state diagram of TVG VHDL code.

The analog output voltage range of DAC is from 0 to 3.3V which corresponds to the 14-bits ranging from 0 (00000000000000) to 16384 (11111111111111) values. So, one digital value corresponds to a value of 3.3/16384 = 0.201 mV. As the gain range needs to be set between 0 and 2.9 V, so it is desired to calculate the corresponding value until which the gain will increase.

This is done as (16384/3.3) *2.9 = 14398. Therefore, the digital values have to increase from 0 (00000000000000) to 14398 (11100000111110) to produce the necessary 2.9V and thereafter, become constant and then fall down to 0 and repeat. A new value will be sent after every 16 clock cycles. DAC communicates serially with FPGA using SPI standards. Data is clocked into the input shift register on the falling edge of the serial clock input. A clock frequency of 5MHz is provided to DAC using FPGA's on-board oscillator. A simple state machine shows the various states of DAC's Operation for generating TVG. Every time, the shift register is increased by a value of '4' and then, the *SY NC* is pulled low for starting the Write operation. This value is added 3600 times to reach the maximum digital value of 14398 and when the Sample Count crosses 3600, it goes into Hold State and keeps that value until the time is 100ms.

A. Simulation Using Modelsim

Simulation of selected components was done using the software, ModelSim from Quartus. It was used to visibly check and understand various operations and therefore, helped in solving the problem whenever the intended operation was not performed.

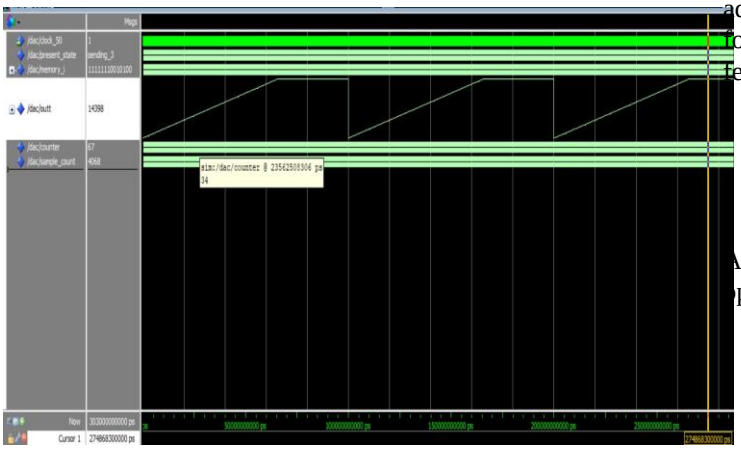

Figure 5: TVG VHDL Simulation using ModelSim

Figure 6 shows different states of TVG VHDL code as described in the state machine before.

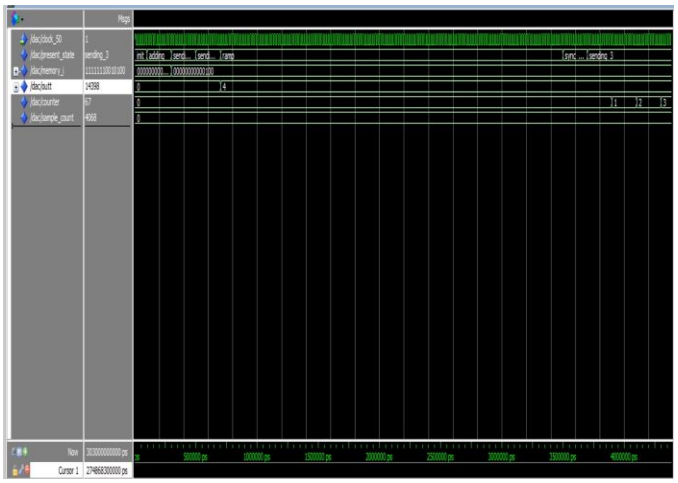

Figure 5: TVG different states.

Conclusion

It was demonstrated that in the front-end receiver, a variable gain amplifier with its channels connected in series can be used for providing the TVG to the incoming pulses with the help of a DAC to vary from 0 to 2.9V. Thus, improving the Signal to Noise Ratio (SNR) and dynamic range. This amplifier, itself offered a very low noise at various gains. Therefore, preventing any additional electronics noise being added to the signal. The variable gain is implemented in the form of ramp wave and is easily controllable, requiring only few modifications when operating at different sea depths.

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